a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate formed over a first one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, at least a portion of said control gate being disposed over a portion of said substrate and being separated from said substrate by said second insulating layer;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said erase gate; and

a source region formed in a portion of said substrate proximate said control gate.

17. (New) A transistor as recited in claim 16 wherein said erase gate is disposed over at least a portion of each of said floating gate and said control gate.

REMARKS

Claims 1-2, 8-10 and 16-17 are now pending. Claims 3-7 and 11-15 have been canceled without prejudice in response to a restriction requirement. New claims 16-17 have been added. Claim 1 has been rejected under 35 U.S.C. §102(b) as being anticipated by Middelhoek et al.(U.S. Patent Number 5,216,269). Claims 8 and 10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chang et al.(U.S. Patent Number 6,126,060). Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Middelhoek et al. in view of Chang et al. Claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. in view of Middelhoek et al. Applicants respectfully traverse each of the rejections as explained below. Claims 1 and 8 have been amended in order to overcome the rejections as explained below. Support for amended claims 1 and 8, and new claims 16-17 is found in the specification of the originally filed application. No new subject matter has been added. Applicants thank the Examiner for careful review of the claims.

The drawings have been objected to under 37 CFR 1.84. Applicants respectfully traverse the objection as explained below.

I. Objections Under 37 CFR 1.83(a)

The drawings have been objected to under 37 CFR 1.84. Applicants note that the drawings originally submitted with the application are informal drawings. In regards to objections to matters of form, Applicants will correct such matters of informality after the allowance of claims, upon submission of formal drawings. Applicants thank the Examiner for careful review of the drawings.

II. Rejections under 35 U.S.C. § 102(b)

Claim 1 has been rejected under 35 U.S.C. §102(b) as being anticipated by Middelhoek et al. Applicants assert that Middelhoek et al. does not disclose an apparatus as now recited in independent claim 1.

Applicants submit that Middelhoek et al. does not disclose a semiconductor device wherein ***"at least a portion of said control gate*** [is] ***disposed over a portion of said substrate and*** [is] ***separated therefrom by said second insulating layer..."*** as now recited in independent claim 1 of the present application. Middelhoek et al. teaches utilizing highly doped boundary regions to separate memory cells from one another in order to reduce the lateral spread of depletion layers and prevent parasitic connections between adjacent memory cells, thereby allowing a more dense placement memory cells on a substrate. No embodiment disclosed by Middelhoek et al. includes a control gate adjacent to the substrate. The present invention minimizes the size of individual memory cells by minimizing the necessary thickness of insulating layers separating various gates within a memory cell.

Therefore, independent claim 1 is patentable under 35 U.S.C. §102(b) over Middelhoek et al. Claim 2 depends from patentable claim 1 and as such incorporate all of the limitations of the independent claim rendering claim 2 patentable also.

III. Rejections under 35 U.S.C. § 102(e)

Claims 8 and 10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chang et al. Applicants assert that Chang et al. does not disclose an apparatus as now recited in independent claim 8.

Applicants submit that Chang et al. does not disclose a semiconductor device wherein ***"at least a portion of...said control gate is disposed over a portion of said substrate and separated***

therefrom by said second insulating layer... as now recited in independent claim 8 of the present application. Chang et al. teaches utilizing the same side wall spacers to define the boundaries of both the floating gate and the control gate, thereby minimizing the poly tunnel oxide thickness. No embodiment disclosed by Chang et al. includes a control gate adjacent to a drain region. The present invention minimizes the size of individual memory cells by minimizing the necessary thickness of insulating layers separating various gates within a memory cell.

Therefore, independent claim 8 is patentable under 35 U.S.C. §102(e) over Chang et al. Claim 10 depends from patentable claim 8 and as such incorporate all of the limitations of the independent claim 8 rendering claim 10 patentable also.

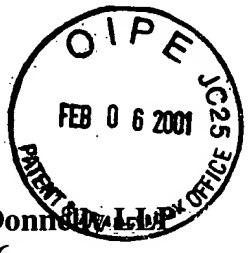
IV. Rejections under 35 U.S.C. § 103

Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Middelhoek et al. in view of Chang et al. Claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. in view of Middelhoek et al. Applicants assert that neither Chang et al., nor Middelhoek et al., either individually or collectively disclose an apparatus as now recited in independent claims 1 and 8.

Applicants submit that neither Chang et al., nor Middelhoek et al, either individually or collectively disclose a semiconductor device wherein ***"at least a portion of...said control gate*** [is] ***disposed over a portion of said substrate and*** [is] ***separated therefrom by said second insulating layer..."*** as now recited in each of the independent claims 1 and 8. Chang teaches a method of manufacturing a memory cell in which the boundaries of the control gate are defined by the same spacers used to define the boundaries of the floating gate, precluding the placement of the control gate adjacent to the substrate.

Applicants assert that claims 1 and 8 as now recited, satisfy the requirements of 35 U.S.C. §103(a). MPEP 2143.03 states that: "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Independent claims 1 and 8 are patentable under 35 U.S.C. §103(a) over Chang et al. in view of Middelhoek et al. Claims 2 and 9 depend from patentable claims 1 and 8 respectively, and as such incorporate all of the limitations of independent claims 1 and 8 rendering them patentable also.

Having fully responded to the outstanding Office Action, Applicants believe that claims 1, 2, 8-10 and 16-17 as amended, are now in condition for allowance, and notice thereof is respectfully solicited. Should a telephone conference be required to expedite the prosecution of this application, the Examiner is respectfully requested to contact the undersigned at the number set out below.



Date: February 2, 2001

Respectfully submitted,

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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) as being deposited on February 2, 2001, with the U.S. Postal Service as First Class Mail in an envelop addressed to: Box Rce Amendment, Assistant Commissioner for Patents, Washington, DC 20231.

Dated: February 2, 2001

Yolette Yturralde-Owen